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Message
Dear Examiner Harrison: Submitted herewith is Response after Final for SN 09/213,748, Inventor: Callway, entitled METHOD AND APPARATUS FOR INDEPENDENT VIDEO AND GRAPHICS SCALING IN A VIDEO GRAPHICS SYSTEM.

Respectfully submitted,
Christopher J. Reckamp, Reg. No. 34,414

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Callway
Serial No. 09/213,748
Filing Date: Dec, 17, 1998
Confirmation No. 6443

Examiner: C. Harrison
Art Group: 2672
Our file no. 00100.98.1319
Docket No. 0100.01319

Title: **METHOD AND APPARATUS FOR INDEPENDENT VIDEO AND GRAPHICS SCALING IN A VIDEO GRAPHICS SYSTEM**

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Nov. 16, 2001 Rosalie Swanson
Date *Rosalie Swanson*

RESPONSE AFTER FINAL

Dear Sir:

Applicants respectfully traverse and request reconsideration.

Claims 1-37 stand rejected 35 U.S.C. §03(a) as being unpatentable over Fujimoto (U.S. Patent No. 5,912,710) (Claim 1 was canceled without prejudice in a previous Response). As to independent Claim 4, in a previous amendment, Applicants pointed out that Applicants' claim, among other things, a video scaler adapted to receive a video stream in a first format, a graphic scaler adapted to receive a graphics data stream in a second format, a merging block operatively coupled to the video scaler and the graphics scaler wherein the merging block combines a separately scaled video stream with a separately scaled graphic stream to produce a video graphics output stream, and a single memory operatively coupled to the graphics scaler and also coupled to the video scaler wherein the single memory further comprises a first memory block and a second memory block. The stream of video data is fetched from the first memory block of the common memory and the stream of graphics data is fetched from the second memory block of a single memory (such as a frame buffer). Accordingly, as noted in the Specification, a frame buffer is more efficiently utilized compared with previous systems.

In the Final Office Action, the Examiner appears to equate the claimed single memory to the DVD itself. For example, the Final Office Action states that although the Examiner admits that Fujimoto fails to disclose the single memory and the two separate memory blocks within the common memory that store separate video information and separate graphics information but agrees that it would have been obvious in view of Fujimoto because Fujimoto teaches storing the separate video and graphics data together on media accessible by the scaling and merging process. However, no column or line number is cited for such a teaching. It appears that the only teaching of storing video and graphics together on a media is the DVD itself (101). However, the DVD is not coupled to the Fujimoto scalers and the DVD does not provide decoded video information that is used by the second scaler of Fujimoto. Accordingly, the attempt at equating the claimed common memory that stores in two different memory blocks separate graphics information to be scaled and the separate video information to be scaled is improper.

In addition, the Office Action appears to misstate the claim language by referring to a "first memory" and to a "second memory": Claim 4 requires a single memory having a first memory block and a second memory block wherein the first memory block has a stream of video from which the video scaler obtains the information and a second memory block that contains graphics data that is fetched from the second memory block for the graphics scaler. The Office Action appears to equate the first memory block to "Fig. 8," "11" (See Final Office Action, p. 2, first full paragraph, line 6). However, Applicants respectfully note that the reference numeral 11 in Figure 8 refers to the CPU and not memory. Moreover, if this was a typographical error and the Final Office Action meant to refer to memory 14, this memory in Figure 8 is a mask ROM and contains the operating system as noted in the Fujimoto reference and does not contain either video or graphics data for scaling. Accordingly, the Final Office Action fails to provide any support for the claimed single memory and associated first memory block and the second memory block.

Moreover, if the Examiner meant to refer to memory block 13 as also having the first memory in the second memory, Applicants respectfully submit that Fujimoto teaches the opposite. For example, Fujimoto teaches that the VRAM 103 contains graphics data that is provided to the first scaler as shown, for example, in Figure 1 (see also Col. 5, ll. 32-36).

Moreover, Fujimoto teaches that the scaled video or video to be scaled is output from the MPEG decoder 102 and is received by scaler 107. As noted in Col. 11, ll. 33-41, Fujimoto states that the main memory 13 includes the video data that is provided to the MPEG2 decoder and that the decoded digital video data under the YCrCb format are sent to the graphics video mixer 203 for blending with the graphics data. Accordingly, the video information to be scaled is not stored in the VRAM 103 and as such is stored in a completely different memory. As such, Fujimoto teaches away from the claimed invention and moreover, does not solve the problem faced by Applicants.

As noted in the Specification (page 6, ll. 11-23), memory in a frame buffer of a videographics integrated circuit can be allocated in a flexible and efficient manner by the claimed invention such that large blocks of memory are not left idle or wasted. Reducing the amount of memory required for either the video or the graphics portion of the display also relieves some of the bandwidth burden on the frame buffer (see, e.g., Specification, p. 14, ll. 12-18). Fujimoto appears to teach an opposite approach. Fujimoto does not appear to teach, among other things, storing the graphics data for scaling in one memory block of memory and storing another assorting video data to be scaled in a different memory block within the same memory that is operatively coupled to the respective scalers. Accordingly, this claim is believed to be in condition for allowance.

Lastly, the "Response to Arguments" section fails to show reference numeral, Fig. or column and line number support that Fujimoto discloses a system storing video and graphics data separately in a single memory where the individual data is provided either selectively or at once to independent scalers that scale the respective data. The "Response to Arguments" section appears to cite Figs. 1, 6 and 7 dealing with the merging of data to produce videographics output. Applicants respectfully request a showing as to where Fujimoto teaches, among other things, the statements referred to in the "Response to Arguments" section of the Final Office Action.

As to Claims 2 and 21, Applicants claim, among other things, wherein the video graphics display engine allocates the size of the first memory block of the single memory and a size of the second memory block of the single memory based on the needs of video data and graphics data. Applicants respectfully reassert the remarks made above with respect to Claim 4 and further note

that the Final Office Action attempts to equate memory controller 122 of Fig. 8 to the claimed controller and that the memory controller 122 allocates memory to the first and second blocks of memory in a common memory wherein the different blocks contain graphics and video data. Applicants respectfully request a showing by column and line number of the videographics scalers in Fig. 8 and the teaching that the memory controller 122 allocates the size of the first and second memory block of a single memory wherein these memory blocks contain separate graphics data and separate video data that are fetched by a graphics scaler and a video scaler. Applicants are unable to find such a teaching with reference to Fig. 8 or within the Fujimoto reference. Accordingly, Applicants respectfully submit that these claims are in condition for allowance.

As per Claims 3 and 22, Applicants respectfully reassert the remarks made with respect to Claim 2 and respectfully note that the alleged merging block of Fujimoto does not appear to be coupled to memory controller 122 as alleged in the Final Office Action. Applicants respectfully note that Claim 3 depends from Claim 2 and that the Final Office Action stated that the controller of Claim 2 was allegedly memory controller 122 which is different from memory controller 201 referenced with respect to Claim 3. The Examiner appears to be taking an inconsistent approach by in one claim alleging that one memory controller is the claimed memory controller whereas the same controller is rejected based on a different memory controller in a dependent claim. In any event, the reference fails to teach or suggest the claim limitations of these claims and therefore these claims are in condition for allowance.

As to Claim 5, the Final Office Action again admits that the Fujimoto fails to disclose first and second memory blocks included in the frame buffer as claimed but then alleges that it would have been obvious to use this disclosure because it teaches providing the data together on media accessible by scaling the merging process as allegedly shown in Figs. 1 and 9. Fig. 1 appears to shown an opposite approach and Fig. 9 deals with the graphics side of the merging process primarily. As noted above, it appears to teach a completely opposite memory approach. Applicants respectfully request a showing by column and line number as to the limitations in Claim 5.

As to Claim 6, Applicants claim, among other things, wherein the controller comprises a video controller operatively coupled to a graphics controller and wherein the video controller is operatively coupled to the video scaler and wherein the graphics controller is operatively coupled to the graphics scaler and wherein the video and graphics controllers are synchronized. The Final Office Action indicates that the video controller coupled to the video scaler and the graphics controller coupled to the graphics scaler is shown in Fig. 1. However, there is no reference numeral indication in the Final Office Action as to what is considered to be the various controllers. Applicants respectfully request a showing.

As to Claim 7, Applicants respectfully reassert the relevant remarks made with respect to Claim 4 and note that this claim is allowable, at least because it depends on an allowable base claim.

As to Claims 8 and 23, Applicants respectfully reassert the relevant remarks made with respect to Claim 4 and note that this claim is allowable, at least because it depends on an allowable base claim.

As to Claims 9 and 11, Applicants respectfully submit that these claims are allowable, at least as depending upon an allowable base claim and since they add additional novel subject matter.

Claims 12 and 25 claim, among other things, a graphics flicker removal block operatively coupled to the graphics scaler wherein the graphics flicker removal block removes flicker from the scaled graphics stream. The Office Action argues that this is allegedly disclosed by the mixer circuit 203 (Applicants note that the Fig. 16 shows 203 as an audio controller but that the patent in Col. 14 refers to the graphics video mixer as 203). Applicants respectfully submit that Fujimoto appears to be silent as to flicker removal blocks for a graphics stream and respectfully request a showing as to any mention of such structure. The Final Office Action alleges that it would have been obvious to have the claimed graphics flicker removal block because Fujimoto teaches a filter having a delay circuit and selectable characteristics. Applicants respectfully note that the cited portion, namely Col. 16, ll. 56 et seq. do not appear to mention a filter having delay circuit used to remove flicker. Since the reference does not appear to teach the claimed circuit,

Applicants also respectfully request the teaching of the motivation to modify Fujimoto since it appears to come from Applicants' own Specification.

As to Claims 13 and 14, the Final Office Action cites the same rejection as to Claim 12. However, Applicants respectfully note that these require a video flicker removal block coupled to the video scaler. The cited portions of Fujimoto to the extent they are relevant refer to the graphics data and as such appear to be silent as to video flicker. Accordingly, these claims are also believed to be in condition for allowance.

As to Claim 14, the Final Office Action admits that Fujimoto fails to disclose a plurality of graphics scalers wherein each of the graphics scalers receives the graphics data stream and scales of graphics images in the graphics data stream based on a ratio between the graphics images and the second format and now put graphics image to produce corresponding scaled graphics streams. The Final Office Action, however, indicates that it would have been obvious to provide such systems because Fujimoto allegedly teaches using a graphics scaler supplying the scaled data in one of two formats. Applicants respectfully request a showing of where Fujimoto indicates that the two formats are done by different graphics scalers. Typically, the formatting is done prior to scaling and as such even if more than two formats were required, a single graphics scaler could be used as taught by Fujimoto. Applicants respectfully submit that Fujimoto is completely silent as to the claimed invention and that it is Applicants' own disclosure which has been used to render the claims obvious and as such this rejection is improper. Accordingly, this claim is also believed to be in condition for allowance.

As to Claim 15, this claim is believed to add additional novel subject matter and is also allowable as depending from an allowable base claim.

As to Claim 16, this claim is believed to add additional novel subject matter and is also allowable as depending from an allowable base claim.

As to Claims 17 and 28, , this claim is believed to add additional novel subject matter and is also allowable as depending from an allowable base claim.

As for Claims 18 and 29, the Final Office Action cites a graphics decompression block in Col. 15, ll. 10 et seq. Applicants respectfully disagree. The cited section actually refers to

graphics data stored in 8 bits per pixel where the data bus from the VRAM is 32 bits. As such, target lines are read out alternately at a unit size of 4 pixels. The bits per pixel are not decompressed. Accordingly, Applicants respectfully request a showing of a graphics decompression block as claimed.

As to Claim 19, Applicants respectfully submit that this claim is allowable for at least being dependent upon an allowable base claim.

As to Claim 20, Applicants respectfully reassert the relevant remarks made with respect to Claim 4.

As to Claim 26, the Final Office Action cites Col. 6, ll. 45-48 and ll. 54-58. However, there does not appear to be a description of a plurality of selected video formats to produce a plurality of scaled video streams. Accordingly, this claim is also believed to be in condition for allowance.

As to Claim 27, Applicants respectfully reassert the relevant remarks made above with respect to Claim 26.

As to Claim 30, Applicants respectfully reassert the remarks made above with respect to Claim 20 and to Claim 4.

As to Claim 31, Applicants respectfully note that the claim requires, among other things, a plurality of video scalers that produce a scaled video data stream of a plurality of video data streams independent from other scaled video streams as well as a plurality of graphics scalers that also produce scaled graphics streams of a plurality of scaled graphics data streams independent from the other scaled graphics data streams and a plurality of merging blocks. Fujimoto is silent as to providing a plurality of video scalers or graphics scalers and as such, Applicants respectfully submit that it appears that impermissible hindsight was used. The Final Office Action cites Col. 16, l. 19 indicating that Fujimoto teaches dynamically changing control data to provide a plurality of graphics and video data to independent graphics and video scalers to scale the respective data and to merge the respective data. However, the cited teaching merely teaches the changing of the filtering characteristics of a videographics mixer. It does not teach controlling a plurality of graphics and video data to independent graphics and video scalers. A

plurality of graphics scalers or video scalers does not appear to be contemplated by Fujimoto. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance.

As to Claim 32, Applicants respectfully reassert the remarks made above with respect to Claim 31.

As to Claim 33, the Final Office Action cites Fig. 9 but no specific block or section of the patent is cited. Applicants again are unable to find any reference to the claimed plurality of memory blocks wherein each of the plurality of memory blocks stores at least one of video data and graphics data wherein these memory blocks are coupled to a plurality of video scalers and separate graphics scalers which are in turn coupled to a plurality of merging blocks. Applicants also respectfully reassert the relevant remarks made with respect to Claim 4. Accordingly, this claim is also believed be in condition for allowance.

As to Claim 34, Applicants respectfully reassert the relevant remarks made above.

As to Claims 35, 36 and 37, Applicants respectfully reassert the remarks made above with respect to Claim 31.

Based on the above remarks, Applicants respectfully submit that the claims are in condition for allowance. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a conference would expedite the prosecution of the instant application.

Respectfully submitted,

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Date: November 16, 2001

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